REMARKS

Claims 1-14 are all the claims presently pending in the Application. Claims 1, 2, 4, 6, 8, and 12 stand objected to for informalities. The disclosure stands objected to for informalities. The disclosure has been amended to overcome the informalities and Applicant requests the Examiner to enter these amendments. These claims have been amended to overcome the informalities and Applicant requests the Examiner to enter these amendments. Claim 8 stands rejected under 35 USC 112, second paragraph; claims 1-3, 5-7, and 9-11 stand rejected under 35 USC 102(e) as anticipated by Chan; claims 4, 8, and 12 stand rejected under 35 USC 103(a) and being unpatentable over Chan in view of Ravinovitz; and claims 13-14 stand rejected under 35 USC 103(a) and being unpatentable over Chan in view of Craddock.

It is noted that any claim amendments are made to merely clarify the language of each claim, and not for distinguishing the invention over the prior art, narrowing the claims or for any statutory requirements of patentability. It is further noted that, notwithstanding any claim amendments made herein, Applicant's intent is to encompass equivalents of all claim elements, even if amended herein or later during prosecution.

The rejections are respectfully traversed in view of the following discussion.

THE CHAN REJECTION

The Examiner alleges that bridge 410 in Figure 4 of the hybrid switching module of Chan that is connected between the Crossbar Switch and Arbiter and the PCI main bus connection discloses the claimed bridge connected between the switch and the data bus connector in claim 1. However, this is respectfully incorrect because the bridge 410 of Chan is located in the wrong place on the HSM, which is a critical difference in operation of the claimed PCM card bridge as compared to the HSM and the operation of bridge 410. Chan's bridge in Figure 4 and the orientation of backplane connections in Chan Figure 1 fail to teach or suggest "a data bus connector for connecting the PCI-based mezzanine card (PMC) to a data bus of a circuit card," and "a bridge, connected between the switch and the data bus connector," as recited in claim 1.

Chan's bridge 404 is located between crossbar switch 408 and a PCI main bus 404. In Chan's Figure 1, HSM A (104) is connected to two PCI busses, the cPCI backplane Bus A 106 is the same as the PCI main bus 404 in Figure 4. Bus 106 allows user cPCI peripheral cards to be connected to the HSM through bridge 410. The PCI bus connection 402 in Chan is not connected to crossbar switch 408 through a bridge. The bridge 404 is placed in between switch 408 and PCI backplane bus 106 so that the bridge "translates signals from the single board computer into signals on the PCI or CPCI bus. As a result, all of the PCI peripheral slots 108, 120 and the user rear

input/output devices 110, 122 are selectively available to each of the single board computers 102, 116." (Chan, C. 4, L. 4-8) Chan's device is intended as a "backup" or "redundant" implementation for a personal computer. (Chan, C. 1, L. 5-10) Thus, the result of Chan's architecture is for accessing the peripheral PCI slots of a personal computer "because each of the single on board computers 102, 116 is able to connect to each of the PCI Peripheral slots 108, 120 and each of the user PCI input/output devices 110, 122...." (Chan, C. 4, L. 19-22)

The bridge of the claimed invention uses a data bus to connect the switch to a circuit card that is located on the PCI-based mezzanine card (PMC), not to a remote circuit card located on a different bus as is the case in the HSM 104/400 of Chan connecting the switch 408 to bus 106 to a data bus 106 off of the HSM. The claim 1 recites that the PCM card comprises the data bus (on the PCM) to a circuit card that would also reside on the PCM. The PCM card is a device in itself, as the Examiner has acknowledged in alleging the comparison to HSM. Thus, alleging that the on-board bus is similar to any external bus connected to the card from anywhere does not have any definitive limiting scope of meaning. According to the claim, the PCM card could be connected via the switch to numerous other PCM cards each having busses over the fabric network, but that is not the same as an architecture of the card itself. The claimed PMC card is used in a network for switching to be distributed through the network fabric as shown in Figure 2 of the Application. Furthermore, due to the claimed switch being a part of the PMC, the claimed bridge is also part of the PMC card that

connects **between** the switch and the data bus of a circuit card. The claimed PCM card has only one bus and that on-board bus is connected to a switch via a bridge. Chan's HSM likewise could be connected to numerous other busses 106 118 that is off-card, but that is not the same meaningful scope as the HSM itself. Chan connects directly to busses in a different way using a different architecture on the HSM than used in the claimed PCM. Thus, Chan does not connect a data bus that is part of the PCM with a bridge that is also part of the PCM card and therefore Chan's architecture is far different and serves a different purpose than the claimed PCM card.

The rejections to claims 2 and 6 over Chan fail for the same reasons. The Examiner has alleged that Chan's architecture for the HSM bridge 410 that is connected between the switch and PCI main bus connection 404 of Figure 4 anticipate the claimed invention. This is incorrect further regarding claim 2 because that claim states that the PCM card is connected to the circuit card and to *the bus for access to the processor of the circuit card* via the bridge that is connected between the switch and the circuit card bus. Chan fails to teach or suggest this aspect because HSM bridge 410 is connected to PCI bus 404, not to the SBC 210, 212 via PCI bus 402. Likewise, Chan's architecture does not teach or suggest Claim 6 where "each PCM bridge can bridge data transfer from each processor (on a circuit card) between each circuit card's bus and each PMC switch. The crossbar switch of Chan's HSM connects to the external bus 404 through bridge 410, not to an on-board circuit card with a processor. No bridge of Chan connects the switch to the circuit card bus and a

processor on the on-board circuit card.

THE REJECTION TO RAVINOVITZ

The Examiner alleged Chan would have been combined with Ravinovitz to produce claims 4, 8, and 12 of the present invention for the advantage of providing root node and leaf node features, wherein said root node supports an initiation of network resets (i.e. fabric resets) and enumeration. Applicant asserts that Chan would not have been combined with Ravinovitz as alleged. Ravinovitz "invention is a peripheral data storage subsystem for use with a computer system that has a host PCI bus and a serial PCI bus adapter coupled to the host PCI bus." (Rav. [0030]) It discloses an array of disks JBOD or RAID configuration that can serve any quantity of external disk storage devices (Rav. 0057]) and that it can use StarFabric implementations with edge nodes and switches, where edge nodes are the connection between the fabric and other protocols or devices (Rav. [0069]). However, Ravinovitz is using a bridge chip and fabric network to support an peripheral array of hard disks. Chan is using the HSM module with a bridge to a PCI bus to support peripherals on a PCI bus where peripheral cards can be inserted. (Col. 3, L. 35-40) Chan's SBC's are used as backups of one another, not for backups of a resource onto an array of drives (Col. 4, L. 12-13).

There is no motivation or suggestion in the references to urge the combination as alleged. There are many ways to hook up hard drives, SBC's and PCI busses, and simply because one disclosure uses one architecture for one purpose and another disclosure uses another architecture for a different purpose is not a reason to combine.

The prior art references themselves should suggest the desirability, and thus the obviousness, of making the combination, independent of the present Application. Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching, suggestion or incentive supporting the combination.

Appellant respectfully submits that these references would not have been combined as alleged by the Examiner. However, even if combined the combination would not teach or suggest each and every element of the claimed invention.

The claimed invention is for a PMC card using a bridge that comprises an edge node that is a terminating point for data signals received from the network fabric through the switch, as recited in claims 4, 8, and 12. Neither Chan nor Ravinovitz have a PMC card using a bridge that has a terminating point for data signals at the bridge. Chan uses its bridge 410 to access external PCI bus 404/106, not for terminating points of data signals from a network fabric. Therefore, the combination does not teach or suggest the claimed invention.

THE REJECTION TO CRADDOCK

The Examiner asserts that Craddock would have been combined with Chan to produce claims 13 and 14. Applicant asserts that Craddock would not have been combined with Chan because while appearing similar, single board computers 102 on a PCI-IB migration connection of Chan are not the same technology and not compatible

with the distributed processing disclosed in Craddock. Chan is concerned with creating a backup hardware system (Col. 1, L. 5) using single board computer systems (col. 2, L 24-25). Distributed processing uses a plurality of processing CPU's to accomplish one or more tasks, but no redundant or backup systems are designed in the architecture. In other words, in distributed processing, there is a single operating system using the power of multiple processors to accomplish tasks faster. The system itself is not backed up or duplicated for redundancy. Thus, neither Chan nor Craddock suggest that a combination of one or the other's architectures would be combined together. Further, one skilled in the art knows that these two architectures are not the same. The prior art references themselves should suggest the desirability, and thus the obviousness, of making the combination, independent of the present Application. Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching, suggestion or incentive supporting the combination.

However, even if combined, the combination would not teach or suggest the claimed invention. The Examiner alleges the virtually contiguous memory space, the bus system 134 of Fig. 1 and the host processor node 102 using a portion of a memory region or portion of a memory window that are mapped to CPUs 136-140 on a different host processor node of Fig. 1 in Craddock disclose the claimed invention of claims 13-14. However, these aspects of Craddock merely disclose direct, RDMA mapping a processor memory region as the memory region of another processor (Craddock [0062]). Craddock uses the memory send and receive pairs in Fig. 5 to map memory to

other processors in the distributing processing network. The DMA mapping of one processor's memory to another processor's memory, even with packets traveling through a fabric network, does not teach or suggest a data bus space of a first circuit card having memory blocks mapped to a processor on a second circuit card, as recited in claim 13. In the claimed invention, the space on the bus of the PMC card is mapped to another processor in the fabric network. This is to allow multiple single board computers to be added to the PMC and provide each of the single board computers the ability to read and write to a data space on the bus space that is routed to another processor. This is not reading and writing directly from processor-to-processor themselves. This is described in the specification as an advantage to scalability. In the distributed processing system of Craddock, each processor must be programmed to map to each other processor in Fig. 5. In the claimed invention, any circuit card can be added to the PMC and the card can read and write to other processors simply by reading and writing to a bus space. No process pairs of Craddock are needed nor are they desired in the claimed invention, since one of the goals of the present invention is to provide cards for expansion on a PMC to another PMC, not distributed processing of a bulk of processors on the same platform.

CONCLUSION

Applicant has revised specification and claims to overcome the objections and 35 USC 112 rejection. Applicant requests the Examiner to enter these amendments.

In view of the foregoing, Applicant submits that claims 1-14, all the claims

presently pending in the Application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above Application to issue at the earliest possible time. The Commissioner is hereby authorized to charge any fees associated with this communication to Attorney's Deposit Account No. 50-1768.

Respectfully Submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: the Commissioner for Patents, United Stated Patent and Trademark Office, PO Box 1450, Alexandria, VA 22313-1450 on June 19, 2006.

Kendal Sheets 6-19-06
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